<u>REMARKS/ARGUMENTS</u>

After the foregoing Amendment, claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36 and 38-54 are currently pending in this application. Claims 9, 19, 29, and 52-54 are amended.

<u>Request for Withdrawal of the Finality of the Office Action</u>

The Applicants respectfully request that the Examiner withdraw the finality of the Office Action mailed on July 20, 2010 because a Request for Continued Examination pursuant to 37 C.F.R. 1.114 is filed along with this Reply.

<u>Claim Rejections - 35 USC § 103</u>

Claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36 and 38-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,150,361 to Wieczorek et al. (hereinafter Wieczorek) in view of 5,333,175 to Ariyavisitakul et al. (hereinafter Ariyavisitakul).

As previously argued, Wieczorek teaches only two power levels, on and off. The portions of Wieczorek upon which the Examiner relies is reproduced below.

> According to the invention, the communication unit may be made to function <u>in one of two operational mode</u>: a low power or energy saving mode and a high power or non energy saving mode. (*See Wieczorek, column 5, lines 4-7, emphasis added.*)

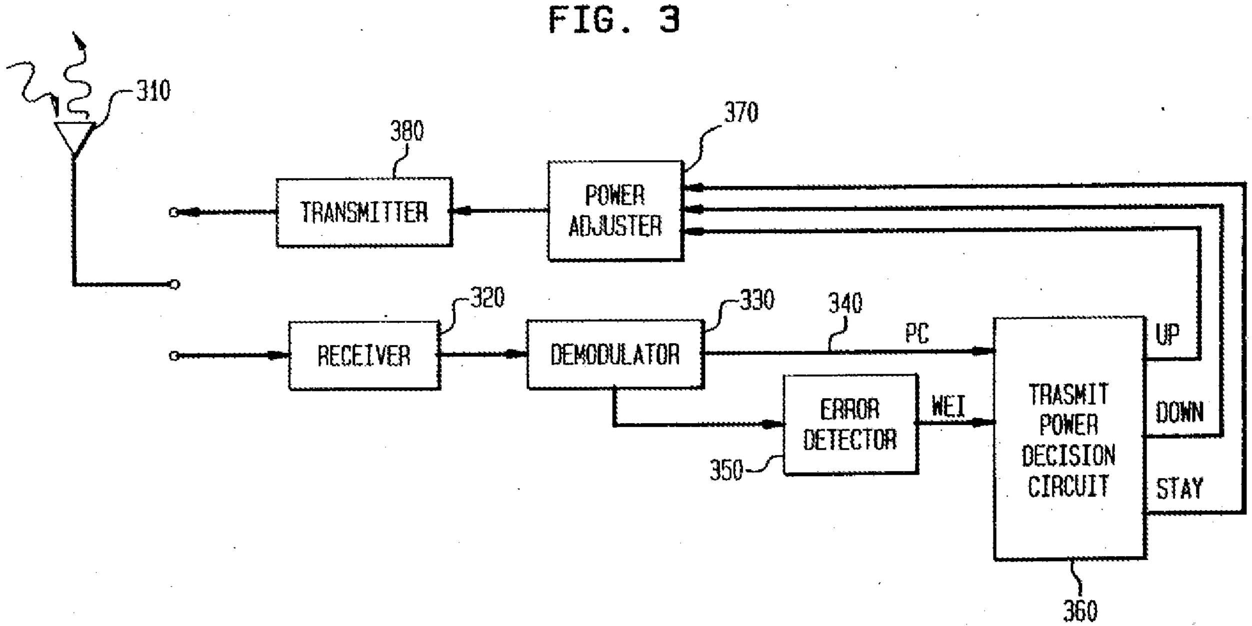
Wieczorek further defines operation of various device components (i.e. circuits) in the "low power or energy saving mode" introduced above as follows.

> In order to conserve energy, the controller 320 periodically <u>deactivates</u> non-essential circuits…(*See Wieczorek, column 4, lines 45-47, emphasis added.*)

As acknowledged by the Examiner, Wieczorek does not specifically disclose a *third signal processing state having an intermediate power consumption level*, as claimed in claim 9. The Examiner relies on Ariyavisitakul as teaching this element.

Independent claims 9, 19, and 29 have been amended to incorporate subject matter previously claimed in dependent claims 52-54, respectively. In the July 20, 2010 Office Action, the Examiner rejected claims 52-54 over Wieczorek in view of Ariyavisitakul stating that Figure 3 and column 15 line 56 to column 16 line 28 of Ariyavisitakul, reproduced below, teaches the claimed features (*see July 20, 2010 Office Action, page 12*).

FIG. 3



A block diagram of the portable unit that adjusts its power output in response to the received power control bit, PC, is shown in FIG. 3. <u>In FIG. 3 antenna 310 receives the downlink signal from the port and directs same to a receiver 320 which is tuned to the downlink carrier frequency</u>. <u>The received analog signal is then input to a demodulator</u> 330 which extracts therefrom the digitized data that forms each downlink TDMA burst. Demodulator 330, as demodulator 230 in FIG. 2, operates using coherent QPSK demodulation with differential decoding to produce a demodulated data burst. Demodulator 330, like demodulator 230, could comprise circuitry of the type described in the aforenoted U.S. Pat. No. 4,941,155 to J. C. Chuang and N. R. Sollenberger.

<u>The power control bit, PC, transmitted with the burst,</u> is extracted from the demodulated bit stream on lead 340. The demodulated bit stream is also input to an error detector 350, which is a similar circuit to error detector 250 in FIG. 2. The output of error detector 350 is a word error indicator, WEI, which is an error flag indicating whether a codeword contained within the burst has been received in error. The WEI and <u>the power control bit are input to a transmitter power decision circuit 360. Based upon the PC</u> and the WEI, <u>decision circuit</u>

> <u>360 decides whether the uplink power should be increased, decreased or remain the same</u>. Specifically, if the WEI indicates an error condition, the PC transmitted by the port may also be in error. A decision is thus made to maintain the uplink power at its previous level. If, however, WEI is ZERO, indicating no detected error, the value of PC controls the decision process. Specifically, if PC is ONE a decision to increase the power is made, and if PC is ZERO a decision to decrease the power is made. The UP, DOWN, and STAY outputs of decision circuit 360 are connected to power adjuster 370, which is connected to transmitter 380. <u>In response to the PC bit and WEI each frame, one of these outputs is energized and power adjuster 370 in response thereto increases, decreases, or maintains the transmit power level of transmitter 380</u>. (*Emphasis added.*)

The Examiner states that the above cited portions of Ariyavisitakul "read as the high power signal processing state and intermediate power signal processing state based on the dynamically adjustment (up/down of the supply power…" However, the cited portions of Ariyavisitakul teach varying transmission power of a transmitter based on a received power control bit. In order to be receiving the power control bit in Ariyavisitakul, the portable unit must be actively receiving an analog signal. The cited portions of Ariyavisitakul therefore only disclose adjusting transmit power of the transmitter when the portable unit is actively receiving an analog signal. In other words, the portable unit of Ariyavisitakul is in a single, particular operating state. There is no teaching in Ariyavisitakul that the operating state of the portable unit changes.

In contrast, claim 9 as currently amended recites, in part, *wherein the plurality of circuit components are configured to operate in a first set of signal*

processing states <u>*associated with a first operating state*</u>*, and in a second set of signal processing states* <u>*associated with a second operating state*</u>*, wherein the first set of signal processing states and the second set of signal processing states are different* (emphasis added). Operating states are discussed in, at least, paragraphs [0126] through [0136] of the present publication.

Since the cited portions of Ariyavisitakul only teach varying a transmission power of a single circuit component (a transmitter) in the context of a single operating state, Ariyavisitakul and Wieczorek taken together at best teach a single operating state wherein a single circuit component is capable of varying power levels. The combination does not teach *a plurality of circuit components…configured to operate in a first signal processing state having an on power consumption level, a second signal processing state having an off power consumption level, and a third signal processing state having an intermediate power consumption… wherein the plurality of circuit components are configured to operate in a first set of signal processing states associated with a first operating state, and in a second set of signal processing states associated with a second operating state, wherein the first set of signal processing states and the second set of signal processing states are different* as claimed in claim 9.

Claims 19 and 29 recite similar limitations to claim 9, and are therefore also patentable over Wieczorek and Ariyavisitakul, either alone or in combination.

Claims 10-12, 14-16, 18, 20-22, 24-26, 28, 30-32, 34-36, and 38-51 depend from claims 9, 19, and 29.

Claims 52-54 have been amended to recite that *the first operating state and the second operating state are each associated with a call state of the processor*. "Call state" is described in, at least, paragraphs [0126] through [0136], and particularly [0126].

Withdrawal of the 35 U.S.C. 103(a) rejection of claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36 and 38-54 is requested.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephonic interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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